REMARKS

Claims 1-4 and 7-22 are in this application and are presented for consideration. By this amendment, Applicant has amended claims 1, 7-9, 12 and 17. Claims 5 and 6 have been canceled and new dependent claims 21 and 22 have been added.

The Office Action states that in considering the patentability of the claims under 35 U.S.C. 103(a), the Examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. To the best of Applicant's knowledge, the subject matter of the various claims was commonly owned at the time the invention was made.

Claims 1-4 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Myers et al. (U.S. 5,400,950) in view of Gotman (U.S. 4,404,453).

The present invention relates to a process for producing a contact structure for connecting two substrates. The process comprises the step of applying solder material to terminal areas of a first substrate to form electrically conductive spacing metallizations with the solder material. The spacing metallizations are in direct contact with the terminal areas of the first substrate. The process further comprises the step of bonding the first substrate with a second substrate. The bonding between the terminal areas of the first substrate and a contact surface area of the second substrate includes partially fusing the spacing metallizations during the bonding action such that a portion of the spacing metallizations is connected to the first substrate. The partial fusion of the spacing metallizations advantageously leaves an essential part of the spacing metallizations in its solidified state such that the terminal areas are located

at a spaced location from the contact surface area. The bonding also includes applying a conductive adhesive to the spacing metallizations or the second substrate. This advantageously securely connects another portion of the spacing metallizations to the second substrate. The process advantageously allows a good electrical connection, a good mechanical connection and provides for the necessary spacing with a simple and effective procedure. The prior art as a whole fails to disclose such features or advantages.

Myers et al. relates to a method for controlling solder bump height for flip chip integrated circuit devices. A flip chip 12 is mounted to a circuit board, which is represented by a substrate 10. A number of bead-like projections are formed on one surface of the flip chip 12 to serve as terminals. These projections electrically interconnect the flip chip 12 to a conductor pattern formed on the substrate 10. The solder bumps 16 are positioned on the flip chip 12 such that, when registered with a conductor pattern on the substrate 10, each of the solder bumps 16 are mated with a corresponding conductor 14. The height of the solder bumps 16 is determined by the effect of a number electrically inactive, dummy solder bumps 20. The solder bumps 20 are positioned on a pad 22 formed on the substrate 10. The solder bumps 16 are deposited on a surface of the flip chip 12 to bond the flip chip 12 to the substrate 10. The flip chip 12 is then soldered to the substrate 10 using a reflow technique which heats the solder bumps 16 and dummy bumps 20 to a temperature above the melting point of the solder alloy.

Myers et al. fails to teach and fails to suggest the combination of connecting one or more spacing metallizations to a second substrate via a conductive adhesive that is applied to one of the spacing metallizations and the second substrate. Myers et al. merely discloses solder

bumps 16 and dummy bumps 20 that are heated above the melting point of the solder alloy in the bumps 16 and 20 such that the solder bumps 16 and dummy bumps 20 are connected to a flip chip 12 and a substrate 10. However, neither the solder bumps 16 nor the dummy bumps 20 of Myers et al. are connected to the flip chip 12 or the substrate 10 via a conductive adhesive as claimed. Compared with Myers et al., solder material of the present invention is applied to terminal areas of a first substrate to form electrically conductive spacing metallizations. A portion of the spacing metallizations of the present invention are partially fused such that the spacing metallizations are connected to a first substrate. According to the present invention, at least one spacing metallization is connected to a second substrate via a conductive adhesive compound. This advantageously provides a simple and effective connection that only requires a partial fusion of the spacing metallizations. This advantageously saves manufacturing costs since only a portion of the spacing metallizations needs to be fused. Myers et al. fails to disclose such manufacturing saving advantages since Myers et al. is completely void of any teaching or suggestion of using a conductive adhesive to connect spacing metallizations to a second substrate as featured in the claimed combination. As such, the prior art as a whole fails to establish a prima facie case of obviousness as Myers et al. does not disclose important features of the present invention.

Gotman discloses bonding a chip 20 and substrate 10 by backwards heating the chip 20 to melt solder globules 22 and 12 arranged on contact pairs 21 and 11. The partial liquidification of solder globules 72 is provided on the contact surface of a first substrate 70 which is to be bonded to chip 60 having solder globules 62. The partial liquidifcation of the

solder globules 72 of Gotman takes place before the partially liquified globules 72 come into contact with the rigid solder globules 62. Upon contact of the partially liquified globules 72 with the rigid solder globules 62 the bonding action takes places in globules 72 being in a liquified state (Column 4, lines 23-31).

Gotman fails to teach and fails to suggest the combination of bonding a first substrate to a second substrate via a conductive adhesive after a portion of each spacing metallizations has been melted to attach the spacing metallizations to the first substrate. Gotman merely discloses bonding a chip 20 and substrate 10 by backwards heating the chip 20 to melt solder globules 22 and 12 arranged on contact pairs 21 and 11. However, the reference is completely void of any teaching for using a conductive adhesive compound for attaching a portion of a spacing metallization to a second substrate. According to the present invention, solder material is applied to a first substrate to form electrically conductive spacing metallizations. A portion of the spacing metallizations is partially fused to connect each spacing metallization to the first substrate. An adhesive is then applied to a second substrate or the spacing metallizations such that each spacing metallization is connected to the second substrate by the conductive adhesive compound. This advantageously allows good electrical connection and excellent mechanical connection between the first substrate and the second substrate. Gotman fails to provide such electrical connection advantages since Gotman is void of any suggestion or teaching for bonding a portion of a spacing metallization to a second substrate via a conductive adhesive as claimed. As such, the prior art as a whole takes a different approach and fails to establish a prima facie case of obviousness since the prior art as a whole does not teach or suggest each

and every feature of the claimed combination.

Claims 5-9, 12-15 and 17-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Myers et al. in view of Gotman and further in view of Leicht et al. (U.S. 5,551,627).

Leicht et al. discloses an electronic assembly 200 comprising solder connection structures 101 of an electronic assembly 100. The electronic assembly 200 includes a portion of a grid array package 206 and a corresponding portion of a circuit board 208 having a solder connection structure 201 disposed therebetween. The solder connection structure 201 interconnects faying surfaces 202 and 204 of the grid array package 206 and the circuit board 208, respectively. The solder connection structure 201 is comprised of a spherical preform 210 composed of a metal alloy solder. The solder connection structure 201 is further comprised of a pair of fillets 212 and 214. The fillets 212 and 214 are a metal alloy solder that is less compliant than the metal alloy solder that comprises the spherical preform 210. The fillets 212 and 214 attach the spherical preform 201 to the respective faying surfaces 202 and 204. A brittle intermetallic layer exists between the fillets 212 and 214 and the respective faying surfaces 202 and 204. To make the solder connection structure 201 more capable of resisting fatigue, the fillets 212 and 214 are tapered so as to focus shear stresses imparted on the solder connection structure 201 to the smallest possible cross sectional area within the solder connection structure 201 and away from the brittle intermetallic layer. The smallest possible cross sectional area of the solder connection structure 201 is not at the brittle intermetallic layer, but rather within the fillets 212 and 214 and at or near the surface of the compliant

spherical preform 210.

As previously discussed above, Myers et al. and Gotman fail to teach or suggest the combination of applying a conductive adhesive to a second substrate or spacing metallizations wherein the spacing metallizations are connected to the second substrate via the conductive adhesive. Leicht et al. also fails to provide any teaching or suggestion for the combination of bonding a first substrate to a second substrate via a conductive adhesive after a portion of each spacing metallizations has been melted to attach the spacing metallizations to the first substrate. At most, Leicht et al. discloses applying a solder paste 312 to a faying surface 202 and applying a solder paste 314 to a faying surface 204 wherein the solder paste 312 and 314 are heated to a temperature above the melting point of the solder paste 312 and 314 to connect a spherical preform 210 to grid array package 206 and circuit board 208. However, Leicht et al. does not disclose spacing metallizations that are connected to a second substrate via conductive adhesive as claimed. Compared with the present invention, Leicht et al. discloses metal-based fillets that are subjected to remelting to connect the solder balls to the circuit board 208 and grid array package 206. The metal-based fillets of Leicht et al. are merely a soldered connection and not a conductive adhesive connection as featured in the present invention. Even assuming the fillets of Leicht et al. are the equivalent of the conductive adhesive as featured in the present invention, Leicht et al. only teaches one and the same kind of connection on both diametrical ends of a spherical preform in order to connect the spherical preform to a grid array package 206 and a circuit board 208. In contrast to Leicht et al., the spacing metallizations of the present invention have one portion connected to a first substrate via partial fusion of the spacing

metallizations and another portion connected to a second substrate via a conductive adhesive. Leicht et al. does not direct the person of ordinary skill in the art toward a spherical preform that is connected to two substrates via two different connections. As such, the prior art as a whole takes a different approach and fails to establish a prima facie case of obviousness as the prior art as a whole does not direct the person of ordinary skill in the art toward important features of the claimed combination.

Claims 10, 11 and 16 have been rejected under 35 U.S.C. 103(a) as being unpatetnable over Myers et al. in view of Gotman and further in view of Beddingfield et al. (U.S. 5,710,071). Although Beddingfield et al. teaches a flip-chip semiconductor device that is formed by mounting a semiconductor die to a wiring substrate, the references as a whole fail to suggest the combination of features claimed. Specifically, Myers et al. and Gotman fail to teach or suggest the combination of fusing a portion the spacing metallizations to a first substrate and connecting another portion of the spacing metallizations to a second substrate during bonding of a first substrate and a second substrate. The references do not suggest the invention and therefore all claims define over the prior art as a whole.

Applicant has added new dependent claims 21 and 22 to further clarify the features of the present invention. Specifically new claims 21 and 22 provide that the conductive adhesive is not subjected to a remelting process. Applicant respectfully requests that the Examiner favorably consider new dependent claims 21 and 22.

Further and favorable consideration on the merits is requested.

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Attached: Petition for One Month Extension of Time

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SHOULD ANY OTHER FEE BE REQUIRED, THE PATENT AND TRADEMARK OFFICE IS HEREBY REQUESTED TO CHARGE SUCH FEE TO OUR DEPOSIT ACCOUNT 13-0410.